JVCKENWOOD Corporation

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Development of Image Signal Processing IP*1 "IPSILOS*2"

Also expecting to provide IP to other companies as a technology to realize high-quality videos demanded by various markets

*1: Abbreviation for Intellectual Property; *2: Abbreviation for Intellectual Property of Special Imaging Logical Optimized System

JVCKENWOOD Corporation is pleased to announce that it has newly developed the image signal processing IP IPSILOS. The newly developed IPSILOS is based on the image signal processing SoC*3 FALCONBRID, which has been used in our consumer and professional camcorders, and has enhanced and expanded basic performance. We intend to install this IPSILOS in our products as a technology to improve the image quality of video-related equipment used in various applications such as in-vehicle products, and also provide it to other companies.

*3: Abbreviation for System-on-a-Chip

Background to the project

In recent years, the sophistication of cameras mounted on smartphones has been accelerating, and there is an extremely high market demand for high image quality in video-related equipment, including dashcams, which are one of our core products.

Given this market background, we have developed a new image signal processing IP IPSILOS based on our proprietary image signal processing SoC FALCONBRID, which has contributed to the high image quality performance of our products by utilizing the knowledge and expertise on high image quality cultivated over the years. We intend to install IPSILOS in our various types of video-related equipment. We are also expecting to provide this IP to manufacturers developing signal processing SoCs used in smartphones and other various markets as a technology to realize higher image quality of video-related equipment. Starting with the development of this IPSILOS, we will consider providing our various image signal processing IPs to other companies. We will work with SoC developers to create more image quality enhancement technologies.

Overview of the image signal processing IP IPSILOS

IPSILOS which we have developed is a circuit block commonly called an Image Signal Processor (ISP), a signal processing circuit that mainly receives RGB electrical signals from a sensor module and converts them into Y/C video signals. In addition to installing IPSILOS in our products, we will provide IP as circuit design data and control driver software environment as Software Development Kit (SDK) for a wide range of applications such as licensing and cooperative development with other companies.

This will not only enable semiconductor manufacturers to easily develop SoCs that realize industry-leading high-quality videos by using IPSILOS, but also enable product developers who are supplied with SoCs to develop a wide range of product lineups in a short period of time by setting various video parameters using the SDK.

Overview of the image processing IP IPSILOS specifications

Supported arrangement system	Single plate RGGB Bayer method
Maximum processing resolution	4480 x 2520@59.94 p (16:9) *Up to 4800 horizontal pixels
internal processing speed	Internal synthesis restriction 400 MHz
Maximum simultaneous input	Full HD@59.94 p x 2 ch Full HD@29.97 p x 4 ch
Maximum number of processed bits	Input 24 bits

Output format YUV 4:2:	2 12 bit / 10 bit / 8 bit
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Key features

Camera signal processing system

- · Piecewise linear processing for tone conversion and expansion
- De-Bayer processing using G-pixel correlation detection
- Dynamic white and black pixel defect correction (up to two consecutive corrections in the same color)
- · Linear matrix and 6-axis color correction and yellow-green correction
- · Brightness control with 24-bit HDR gamma processing (HDR: 144 dB)
- · Brightness, color and aperture noise reduction by Hadamard transform
- · High-brightness and low-brightness color suppression processing
- · Optical lens peripheral blur correction processing
- 3DNR processing using horizontal and vertical motion detection
- 480-division variance, histogram, peak value calculation, output summation/average value calculation (AE/AWB/AF)
- · Dynamic gamma processing without load on software using histogram
- Image enhancement correction processing for visually higher contrast

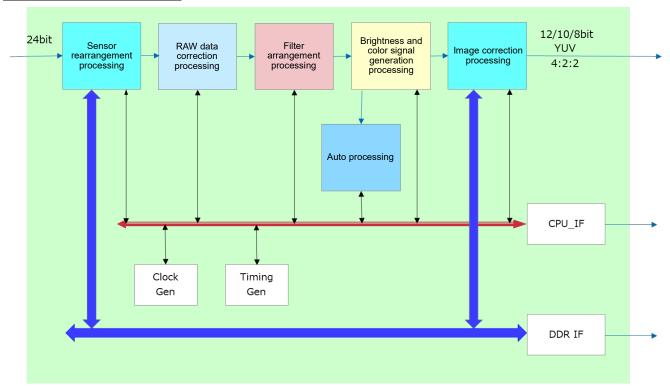
Optical lens correction system

- Shading correction (spline interpolation)
- Distortion correction (SRAM supported)
- Chromatic aberration of magnification correction

Video correction system

- · HDR composition with two shatters
- Flicker correction circuit for fluorescent lamp (indoors, etc.)

Circuit component blocks



Comparison of image quality (1) High Dynamic Range (HDR)

Function	Existing Technology	New IP "IPSILOS"
Tunnel exit		
Buildings at night		

(2) Image correction processing

Dynamic gamma	No correction	New IP "IPSILOS"
This correction automatically generates a gamma curve from histogram information of brightness, and increases the gamma curve of parts where the value is large in the histogram analysis.		

Image	No correction	New IP "IPSILOS"
This correction makes the level difference of the brightness component at the boundary of objects smoother in terms of brightness change over a wide area. The black looks tighter.		

<u>Trademarks</u>
■ "IPSILOS" and "FALCONBRID" are trademarks of JVCKENWOOD Corporation.

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